

ABSTRACT

Methods and apparatus for accessing memory locations in a memory device in different orders. In one implementation, a memory device includes: a memory array, including a plurality of memory locations divided into memory pages, where each memory location has a row address and a column address; a row decoder connected to the memory array for selecting a row address in the memory array; a column decoder connected to the memory array for selecting a column address in the memory array; and a multi-sequence address generator for generating addresses, where the multi-sequence address generator has a burst mode and in burst mode generates one of two or more burst sequences of addresses according to received burst parameters, and where each sequence has an index indicating the separation between two addresses in the sequence.

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